

Signal name

R-type lw sw

beq

inputs op5（26） 0 1 1 0

op4 0 0 0 0

op3 0 0 1 0

op2 0 0 0 1

op1 0 1 1 0

op0（31） 0 1 1 0

outputs RegDst 1 0 x x

ALUSrc 0 1 1 0

MemtoReg 0 1 x x

RegWrite 1 1 0 0

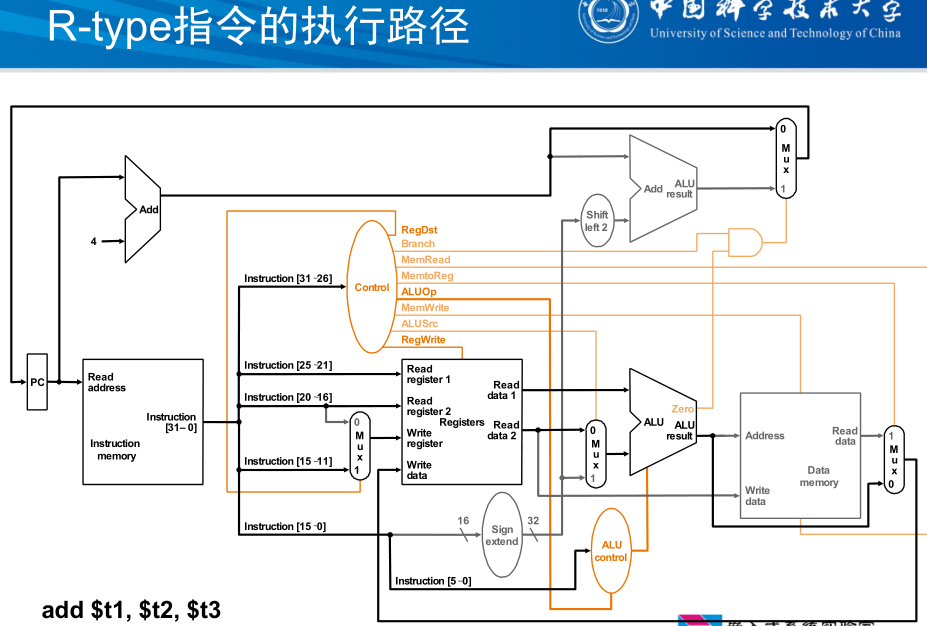
MemRead 0 1 0 0

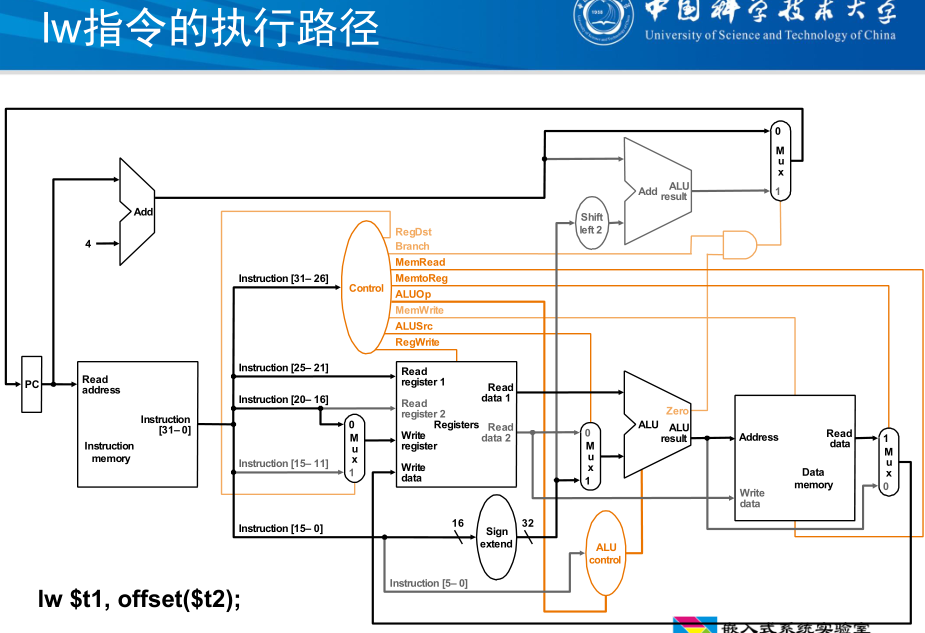
MemWrite 0 0 1 0

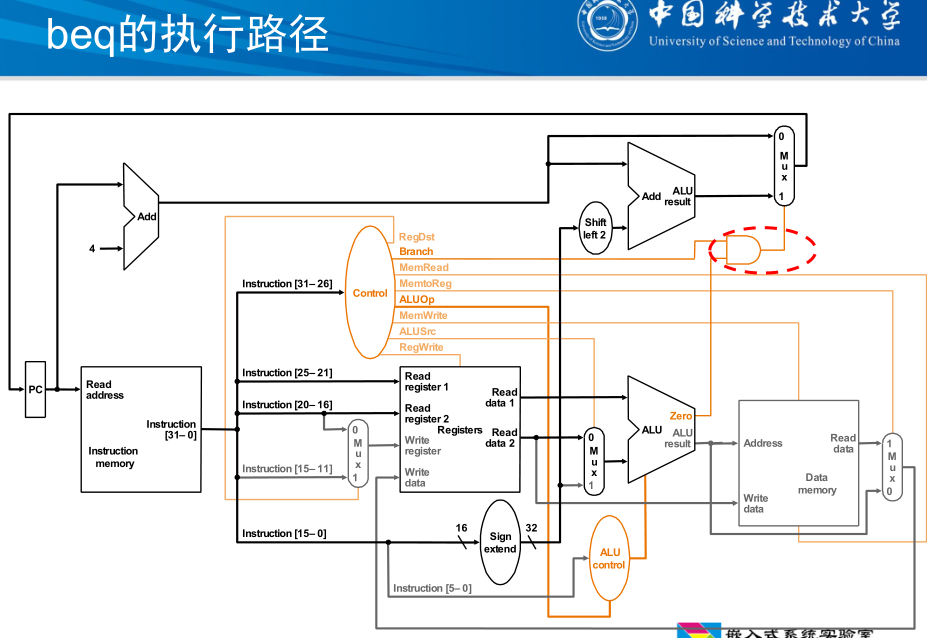
Branch 0 0 0 1

ALUop1 1 0 0 0

ALUop0 0 0 0 1







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